(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
8 February 2001 (08.02.2001)

PCT

(10) International Publication Number
WO 01/09927 A1

(51) International Patent Classification[7]: H01L 21/00, 23/544, 21/66

(21) International Application Number: PCT/US00/16690

(22) International Filing Date: 16 June 2000 (16.06.2000)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/362,976 28 July 1999 (28.07.1999) US

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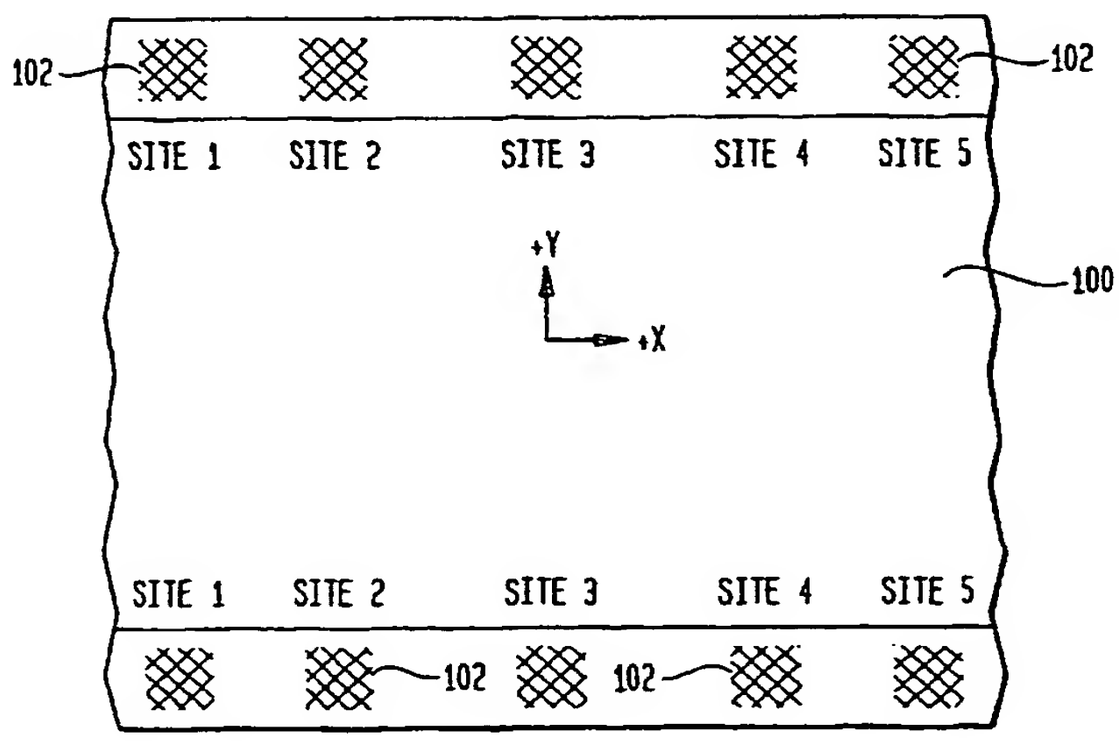
(81) Designated States *(national)*: CN, JP, KR.

(84) Designated States *(regional)*: European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published:
— *With international search report.*
— *Before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments.*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: SEMICONDUCTOR STRUCTURES AND MANUFACTURING METHODS



(57) Abstract: A semiconductor body having an alignment mark comprising a pair of sets of parallel lines disposed on the semiconductor body, the parallel lines in one of the sets being disposed orthogonal to the parallel lines in the other one of the set, the two sets of parallel lines being in an overlaying relationship. Also, a method and apparatus for detecting an alignment mark on a semiconductor body. The method and apparatus provide an alignment illumination comprising a pair of orthogonal, lines of impinging light which is scanned over the surface of the alignment mark, one of such pair of impinging light lines being orthogonal to, and laterally displaced from, the other one of such pair of impinging light lines, impinging light being reflected by the alignment lines in the surface of the semiconductor when such impinging light is over to provide a pair of laterally displaced beams of reflected light. The method includes detecting in each one of a pair of laterally spaced detectors a corresponding one of the laterally displaced beams of reflected light.

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SEMICONDUCTOR STRUCTURES AND MANUFACTURING METHODS

Background of the Invention

This invention relates generally to semiconductor structures and manufacturing methods and more particularly to alignment techniques used therein.

As is known in the art, semiconductor integrated circuits are manufactured using a series of process steps which require proper alignment of the semiconductor wafer. Many alignment systems use reflected light from profile patterns formed on the surface of the semiconductor wafer to determine the location of the wafer. Such an arrangement is shown in FIG. 1. An alignment illumination 10, here a cross, is focused onto the surface 12 of the semiconductor wafer 14 using an optical system 16. A portion of the light is reflected from the surface of the semiconductor wafer is directed by the optical system 16 to a detector arrangement 20. The wafer 14 has formed along one portion thereof an alignment mark 22, here shown diagrammatically as a series of grooves 24 etched into the surface 12 of the wafer 14. As the wafer 14 is scanned horizontally, the detector arrangement 20 produces waveforms which enable detection of the alignment of the wafer 14 relative to the optical system 16.

More particularly, and referring also to FIG. 2, there are shown four sites, i.e., site 1, site 2, site 3 and site 4 of alignment marks on each of both the upper and lower peripheral portions of a semiconductor wafer 14. Each one of the sites includes two sets of lines 13, one at + 45 degrees with respect to the vertical, or Y axis, and the other set of lines 15 being at - 45 degrees with respect to the Y axis. The alignment illumination

projected by the optical system (FIG. 1) onto the surface of the wafer is a cross, such as used in the MICRASCAN equipment manufactured by Silicon Valley Group (SVG), San Jose, CA. A "standard" alignment mark, in one half of a site, for the MICRASCAN III equipment is shown in FIG. 3 and consists of wide stripes at a 45 degree angle separated by variable spacing. Another version is shown in FIG. 4 and is made up of lines at the locations where the "standard" mark has the edges of its stripes. The size of both versions is 60x60 micrometers. The alignment marks etched into the surface of the wafer are shown in FIG. 2 as a pair orthogonal sets of a series of parallel lines, only one of the two sets being shown in FIGS. 3 and 4.

Referring again to FIG. 1, the alignment illumination, a cross is projected onto the surface 12 of wafer 14 with the pair of intersecting arms of the cross being disposed nominally orthogonal to the lines in each of the sites. The cross-shaped light (i.e., the alignment illumination) is projected by the optical system 16 onto, and scanned across the site (FIG. 2) along the X direction indicated on the surface 12 of the wafer 14. The optical system 16 includes a prism (FIG. 1) which directs a portion of the light reflected surface 12 of the wafer 14 onto a detector arrangement 20 shown diagrammatically in FIG. 1. Thus, as indicated, there are four detectors 22_1, 22_2, 22_3, and 22_4; one pair 22_1 and 22_2 being disposed along an axis +45 degrees with respect to the Y axis and one pair 22_3 and 22_4 being disposed along an axis - 45 degrees with respect to the Y axis. The pair of detectors 22_1 (i.e., "Left +45") and 22_2 (i.e., "Right +45") is used for detection of light reflected by lines 13 at +45 degrees with respect to the Y axis and the pair of detectors 222_3 (i.e., "Left -45")

and 22_4 (i.e., "Right -45") are used to detect light reflected by lines 15 at -45 degrees with respect to the Y axis.

More particularly, to determine the location of an alignment site, two marks 13, 15 (FIG. 1); one oriented at + 45 degrees and one at -45 degrees with respect to the Y axis, are required. The alignment marks 13, 15 are scanned by the optical system with an X shaped illumination, as described above. The light reflected from the surface of the wafer and the alignment lines is detected in the dark field mode, i.e., only light scattered from the marks at an angle is analyzed. Two detectors 22_1 and 22_2 record simultaneously the reflected light; one detector 22_2 located to the right side and one detector 22_1 to the left side of the mark's edge. When scanning the + 45 degree lines 13, the set of detectors 22_1 and 22_2 is activated and when the - 45 degree lines 15 are scanned, the set of detectors 22_3, 22_4 are activated.

More particularly, referring to FIG. 1, when the alignment illumination is over the +45 degree lines 13 of site 1, the "Left +45" and "Right +45" detectors 22_1 and 22_2 are activated and the "Left -45" and "Right -45" detectors 22_3 and 22_4, are deactivated. When the alignment illumination moves over the -45 degree lines 15 of site 1, the "Left -45" and "Right -45" detectors 22_3 and 22_4 are activated and the "Left +45" and "Right +45" detectors 22_1 and 22_2 are deactivated. It is noted that with such an arrangement, each alignment site is made up of a pair of spatially separated sets 13, 15 of parallel orthogonal lines with two sets in the site being sequentially activated/deactivated detectors. Such spatial separation increases the area required for an alignment site.

Summary of the Invention

In accordance with the present invention, a semiconductor body is provided having an alignment mark comprising a pair of sets of parallel lines disposed on the semiconductor body, the parallel lines in one of the sets being disposed orthogonal to the parallel lines in the other one of the set, the two sets of parallel lines being in an overlaying relationship.

With such structure, the same amount of wafer surface area enables twice as many alignment sites. Thus, the arrangement allows the alignment system to acquire twice the amount of metrology information during the same alignment scanning process to thereby increase the alignment quality. Further, there is no loss of through-put because the same time is used for scanning the sites as in the system described above.

In accordance with another embodiment, a method is provided for detecting an alignment mark on a semiconductor body. The method includes providing the alignment mark on the semiconductor body, such alignment mark comprising a pair of sets of parallel lines disposed on the semiconductor body, the parallel lines in one of the sets being disposed orthogonal to the parallel lines in the other one of the set, the two sets of parallel lines being in an overlaying relationship. The alignment illumination comprising a pair of orthogonal, lines of impinging light is scanned over the surface of the alignment mark, one of such pair of impinging light lines being orthogonal to, and laterally displaced from, the other one of such pair of impinging light lines, impinging light being reflected by the alignment lines in the surface of the semiconductor when such impinging light is over to provide a pair of laterally displaced beams of reflected light. The method includes detecting

in each one of a pair of laterally spaced detectors a corresponding one of the laterally displaced beams of reflected light.

In accordance with another embodiment of the invention, apparatus is provided for detecting an alignment mark on a semiconductor body, such alignment mark. The alignment mark comprises a pair of sets of parallel lines disposed on the semiconductor body, the parallel lines in one of the sets being disposed orthogonal to the parallel lines in the other one of the set, the two sets of parallel lines being in an overlaying relationship. The apparatus includes an optical system for scanning an alignment illumination comprising a pair of orthogonal, lines of impinging light over the surface of the alignment mark, one of such pair of impinging light lines being orthogonal to, and laterally displaced from, the other one of such pair of impinging light lines, impinging light being reflected by the alignment lines in the surface of the semiconductor when such impinging light is over to provide a pair of laterally displaced beams of reflected light. The apparatus also includes a pair of laterally spaced detectors, each one of the detectors being positioned to detect a corresponding one of the laterally displaced beams of reflected light.

Brief Description of the Drawing

These and other features of the invention will become more readily apparent from the following detailed description when read together with the accompanying drawings, in which:

FIG. 1 is schematic diagram of an alignment system according to the PRIOR ART;

FIG. 2 is a plan view of a semiconductor wafer having alignment marks according to the PRIOR ART etched

into such surface;

FIGS. 3 and 4 are sketches of alignment marks according to the PRIOR ART;

FIG. 5 is a plan view of a semiconductor wafer having alignment marks according to the invention etched into such surface;

FIGS. 6 and 7 are sketches of alignment marks according to the invention; and

FIG. 8 is schematic diagram of an alignment system according to the invention, such system being adapted for use with a semiconductor wafer having the alignment marks shown in either FIG. 6 or FIG. 7.

Description of the Preferred Embodiments

Referring now to FIG. 5, a portion of a semiconductor body 100, here a single crystal silicon body is shown having formed thereon an the alignment sites, five sites (i.e., site 1, site 2, site 3, site 4 and site 5) along the top outer peripheral portion of the wafer and five sites (i.e., site 1, site 2, site 3, site 4, and site 5) along the lower outer peripheral portion. Each one of the sites is identical, an exemplary one thereof being shown in detail in FIG. 6. It is noted that the alignment site includes a single, composite alignment mark 102. The alignment mark 102, as noted above, is formed in a portion of the surface 104 of the semiconductor body 102, here as grooves 106. The surface 104 of the semiconductor body 102 is adapted to reflect light energy impinging on such surface with a predetermined wavelength.

More particularly, the semiconductor body 100 has an alignment mark 102 comprising a pair of sets of parallel lines 112, 114 (FIG. 6) disposed on the semiconductor body 100, the parallel lines 112 in one of the sets being disposed orthogonal to the parallel lines

114 in the other one of the set, the two sets of parallel lines 112, 114 being in an overlaying relationship to provide a composite mark at each one of the sites (FIG. 5).

Apparatus 200 shown in FIG. 8 is provided for detecting the alignment mark 102 (FIG. 6) on a semiconductor body 110. As noted above, the alignment mark 100 comprises a pair of sets of parallel lines 112, 114 (FIG. 6) disposed on the semiconductor body 100. The parallel lines 112, 114 in one of the sets is disposed orthogonal to the parallel lines 112, 114 in the other one of the sets. The alignment mark 102 includes, as noted above, grooves 106 having sidewalls 108 terminating at the surface 104 of the semiconductor body 100, as indicated in FIG. 8. The grooves 106 have bottom portions 110 recessed into the surface portion of the semiconductor body 100. The two sets of parallel lines 112, 114 are in an overlaying relationship. The apparatus 200 includes an optical system 202 for scanning an alignment illumination 204 comprising a pair of orthogonal, laterally displaced, along the X axis, lines 208, 210 of impinging light over the surface of the alignment mark 102. One of the pair of impinging light lines, here line 208, is orthogonal to, and laterally displaced from, the other one of such pair of impinging light lines 210. Here, the line 210 is projected onto the surface of the wafer 100 at an angle of - 45 degrees with respect to the Y axis (FIG. 5) and the line 208 is projected onto the surface of the wafer 100 at an angle of + 45 degrees with respect to the Y axis (FIG. 5). The impinging light (i.e., the alignment illumination) is reflected by the surface of the semiconductor body 100 when such impinging light is over the composite alignment mark 102 to provide a corresponding pair of laterally

displaced beams 211, 213 of reflected light. The apparatus includes a detector arrangement 220. The detector arrangement 220 includes a pair of detectors configurations 220_1 and 220_2. The projected beams 211, 213 are directed by the optical system 200 to the detector configurations 220_1 and 220_2, respectively, as indicated. The detector configuration 220_1 includes a pair of detectors 222_1 and 222_2, shown in FIG. 8. Shown diagrammatically with the detectors 222_1 and 222_2 is the projection of the illumination 210 (i.e., 210') if the surface of the wafer 100 were perfectly flat. Thus, detectors 222_1 and 222_2 are positioned to detect energy reflected by lines 112 (FIG. 6).

In like manner, the detector configuration 220_2 includes a pair of detectors 222_3 and 222_4, shown in FIG. 8. Shown diagrammatically with the detectors 222_3 and 222_4 is the projection of the illumination 208 (i.e., 208') if the surface of the wafer 100 were perfectly flat. Thus, detectors 222_3 and 222_4 are positioned to detect energy reflected by lines 114 (FIG. 6).

With such apparatus, the alignment illumination is scanned over the surface of the alignment mark 102, one of such pair of impinging light lines 108 being orthogonal to, and laterally displaced from, the other one of such pair of impinging light lines 110, impinging light being reflected by the alignment lines in the surface of the semiconductor when such impinging light is over to provide a pair of laterally displaced beams 211, 213 lines of reflected light. The detectors 222_1, 222_2, 222_3 and 222_4 detect in each one of a pair of laterally spaced detector configurations 220_1, 220_2, respectively, a corresponding one of the laterally displaced beams 211, 213 of reflected light. The - 45 degree and + 45 degree oriented alignment lines 208, 210, respectively, of the

cross-shaped alignment illumination 204 are separated locally by at least the width W (FIGS. 6 and 8) of the alignment mark 102. This will result in the alignment mark being scanned first by the + 45 degree line 208 and subsequently by the - 45 degree line 210. This arrangement allows the separation of the alignment detectors 222_1, 222_2 and 222_3, 222_4 for + 45 degree and - 45 degree orientations, respectively. As a result, each signal, or waveform, produced by the detectors can be recorded without background noise from the other line orientation.

Other embodiments are within the spirit and scope of the appended claims. For example, other types of composite alignment marks may be used such as shown in FIG. 7.

What is claimed is:

1. A semiconductor body, comprising:

an alignment mark comprising a pair of sets of parallel lines disposed on the semiconductor body, the parallel lines in one of the sets being disposed orthogonal to the parallel lines in the other one of the sets, the two sets of parallel lines being in an overlaying relationship.

2. A semiconductor body, comprising:

an alignment mark comprising a pair of sets of parallel lines disposed on the semiconductor body, the parallel lines in one of the sets being disposed orthogonal to the parallel lines in the other one of the sets, the parallel lines in the one of the sets crossing the parallel lines in the other one of the sets.

3. A method for detecting an alignment mark on a semiconductor body, comprising:

providing the alignment mark on the semiconductor body, such alignment mark comprising a pair of sets of parallel lines disposed on the semiconductor body, the parallel lines in one of the sets being disposed orthogonal to the parallel lines in the other one of the set, the two sets of parallel lines being in an overlaying relationship;

scanning an alignment illumination comprising a pair of orthogonal, lines of impinging light over the surface of the alignment mark, one of such pair of impinging light lines being orthogonal to, and laterally displaced from, the other one of such pair of impinging light lines, impinging light being reflected by the alignment lines in the surface of the semiconductor when such impinging light is over to provide a pair of

laterally displaced beams of reflected light; and

detecting in a each one of a pair of laterally spaced detectors a corresponding one of the laterally displaced beams of reflected light.

4. Apparatus for detecting an alignment mark on a semiconductor body, such alignment mark, such alignment mark comprising a pair of sets of parallel lines disposed on the semiconductor body, the parallel lines in one of the sets being disposed orthogonal to the parallel lines in the other one of the set, the two sets of parallel lines being in an overlaying relationship, such apparatus comprising:

an optical system for scanning an alignment illumination comprising a pair of orthogonal, lines of impinging light over the surface of the alignment mark, one of such pair of impinging light lines being orthogonal to, and laterally displaced from, the other one of such pair of impinging light lines, impinging light being reflected by the alignment lines in the surface of the semiconductor when such impinging light is over to provide a pair of laterally displaced beams of reflected light; and

a pair of laterally spaced detectors, each one of the detectors being positioned to detect a corresponding one of the laterally displaced beams of reflected light.

FIG. 1
(PRIOR ART)

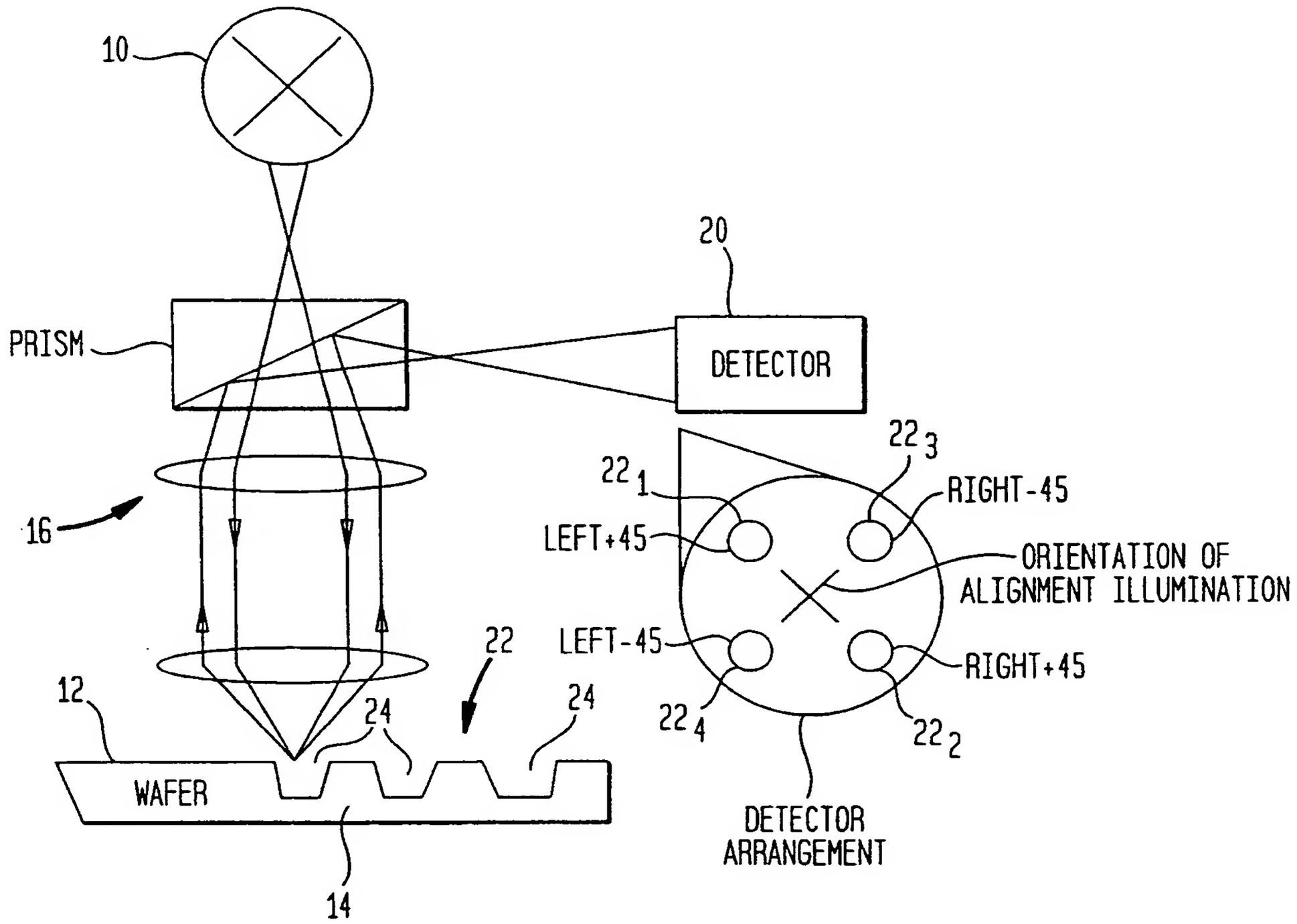


FIG. 2
(PRIOR ART)

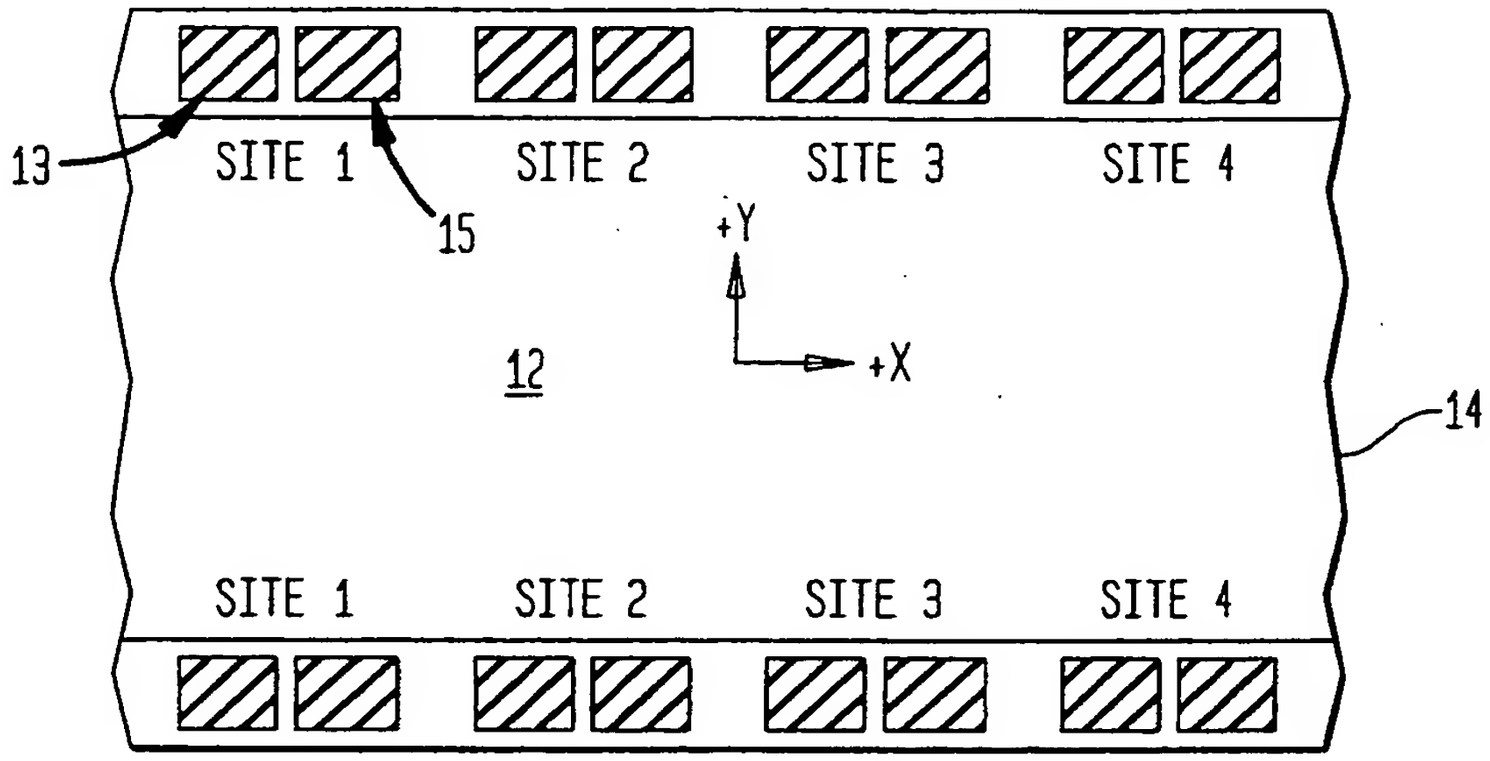


FIG. 3
(PRIOR ART)

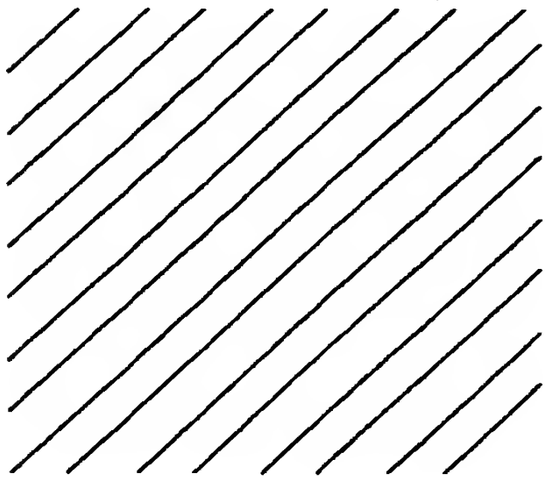


FIG. 4
(PRIOR ART)

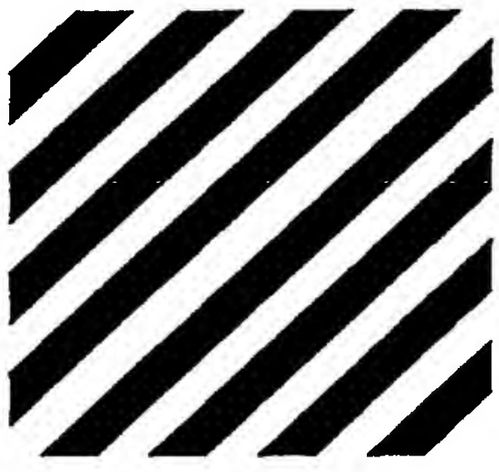


FIG. 5

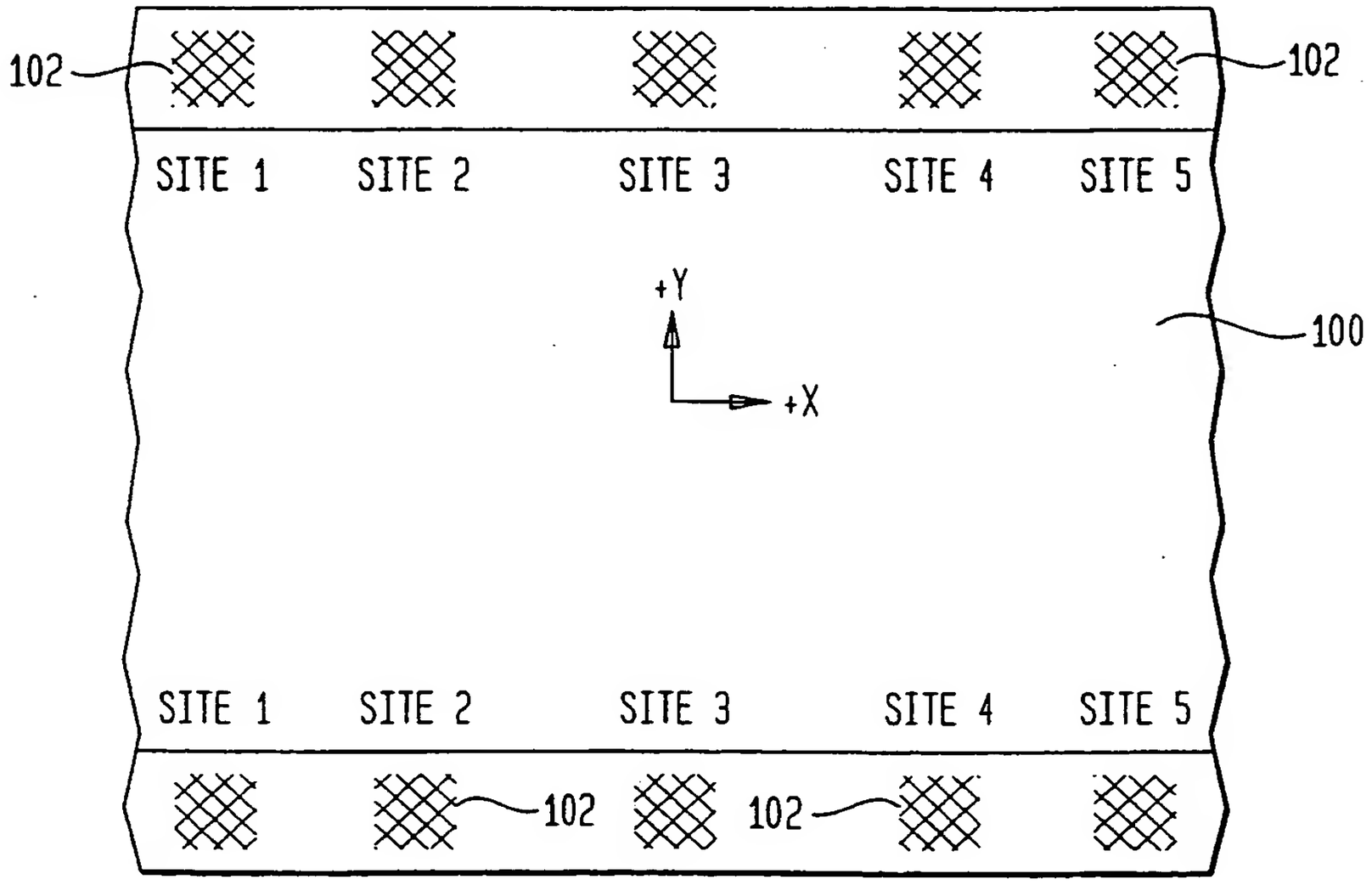


FIG. 6

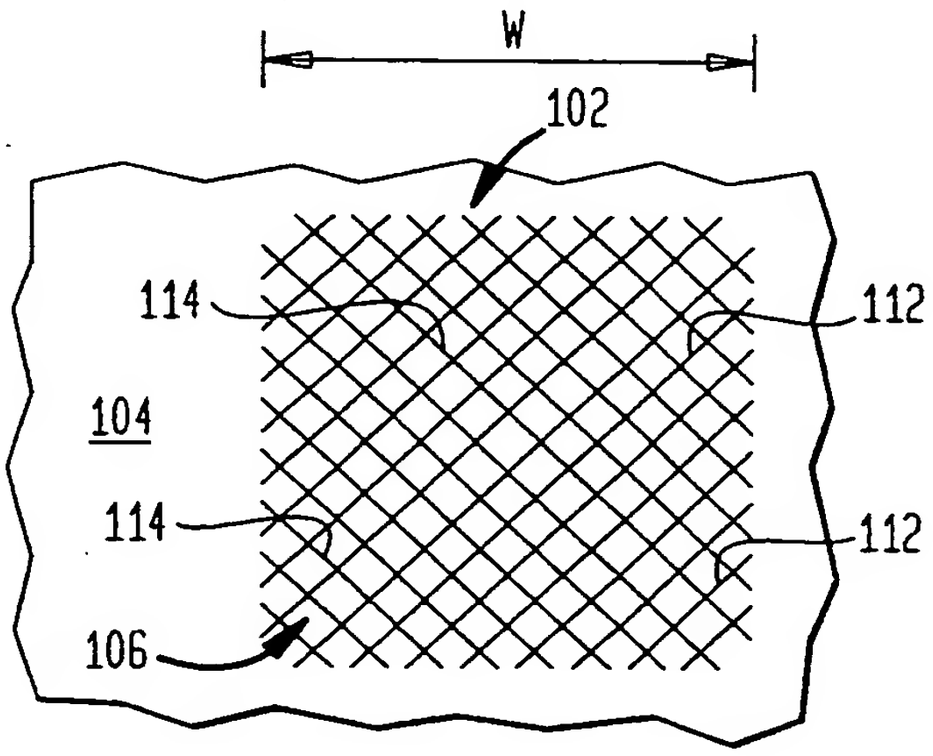


FIG. 7

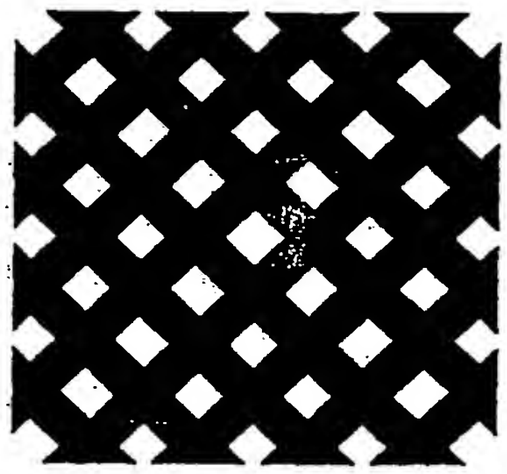
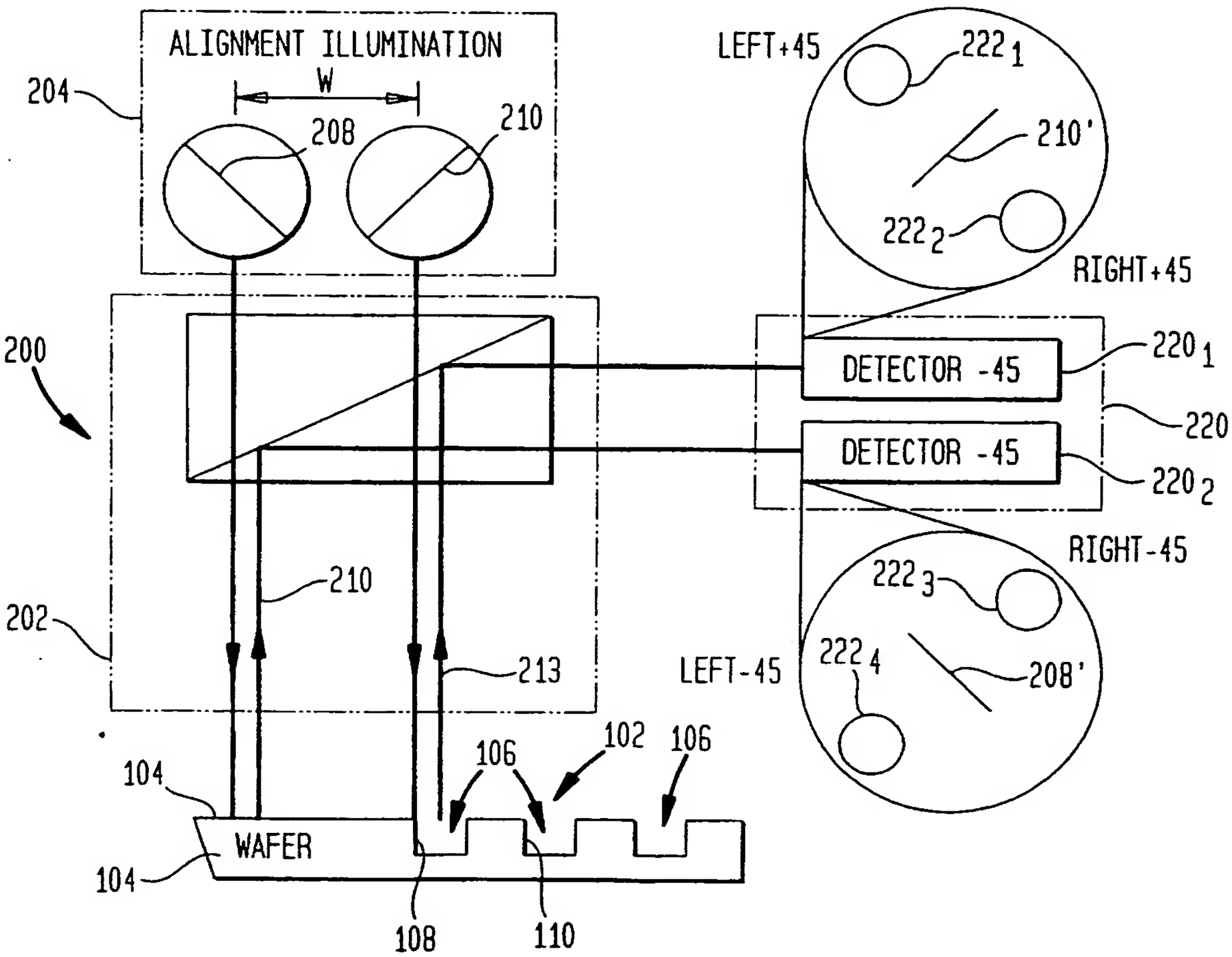


FIG. 8



INTERNATIONAL SEARCH REPORT

Inter nal Application No
PCT/US 00/16690

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L21/00 H01L23/544 H01L21/66

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, PAJ, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 4 932 064 A (KASAHARA TAKESHI) 5 June 1990 (1990-06-05) abstract; claims; figures column 1, line 5 -column 2, line 23 column 3, line 9 -column 4, line 42	1,2
Y	---	3,4
Y	US 3 885 877 A (KOLB GEORGE A ET AL) 27 May 1975 (1975-05-27) column 1, line 4 - line 68; figure 1 column 2, line 34 -column 3, line 58	3,4

X	US 5 095 511 A (OKAZAKI AKIHIRO) 10 March 1992 (1992-03-10) abstract; figure 6A column 6, line 9 - line 29	1,2

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
6 December 2000	20/12/2000

Name and mailing address of the ISA	Authorized officer
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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 3 603 728 A (ARIMURA YOSHIAKI) 7 September 1971 (1971-09-07) abstract; claims; figure 2I column 2, line 18 - line 56	1,2
X	US 5 106 432 A (MATSUMOTO RYOICHI ET AL) 21 April 1992 (1992-04-21) abstract; figure 11 column 1, line 6 -column 2, line 34 column 5, line 4 -column 6, line 20	2

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Form PCT/ISA/210 (continuation of second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Information on patent family members

Interr. nal Application No
PCT/US 00/16690

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 4932064 A	05-06-1990	JP 1826499 C	28-02-1994
		JP 63104348 A	09-05-1988
US 3885877 A	27-05-1975	CA 1012656 A	21-06-1977
		DE 2439987 A	17-04-1975
		FR 2247758 A	09-05-1975
		GB 1481099 A	27-07-1977
		IT 1020143 B	20-12-1977
		JP 967498 C	26-07-1979
		JP 50067584 A	06-06-1975
		JP 54000152 B	06-01-1979
US 5095511 A	10-03-1992	JP 2001107 A	05-01-1990
		JP 2651199 B	10-09-1997
		KR 9302676 B	07-04-1993
US 3603728 A	07-09-1971	DE 1816816 A	14-08-1969
		FR 1597270 A	22-06-1970
		GB 1255502 A	01-12-1971
		NL 6818695 A	01-07-1969
US 5106432 A	21-04-1992	JP 2301121 A	13-12-1990
		JP 2304912 A	18-12-1990
		KR 177148 B	15-04-1999
		US 5128280 A	07-07-1992